

What is claim d is:

1           1. A method of fabricating a semiconductor device having a recess  
2 region in an insulation layer on a silicon substrate, the method comprising  
3 the steps of:

4           depositing a barrier metal on the whole surface of the insulation layer  
5 including the substrate surface in the recess region;

6           depositing selectively an anti-nucleation layer on the barrier metal  
7 except in the recess region;

8           depositing a CVD-Al layer on the barrier metal in the recess region;

9           depositing a metal or a metal alloy for inhibiting aluminum migration  
10 on the barrier metal except in the recess region; and

11          depositing a PVD-Al layer and reflowing the PVD-Al layer.

1           2. The fabrication method of claim 1, wherein the metal or the metal  
2 alloy inhibiting aluminum migration is one of Ti, TiN, Ti/TiN, Ta, TaN and  
3 Ta/TaN.

1           3. The fabrication method of claim 1, wherein a deposition thickness  
2 of the metal or the metal alloy inhibiting aluminum migration is less than  
3 100 Å.

**ABSTRACT OF THE DISCLOSURE**

Sub A-1

204010-2525001

A method of fabricating a semiconductor device having a recess region in an insulation layer on a silicon substrate, comprising the steps of depositing a barrier metal over the entire surface of the insulation layer including the substrate surface in the recess region, depositing selectively an anti-nucleation layer on the barrier metal except in the recess region, depositing a CVD-Al layer on the barrier metal in the recess region, depositing a metal or a metal alloy inhibiting aluminum migration on the barrier metal except in the recess region, and depositing a PVD-Al layer and re-flowing the PVD-Al layer, for improving the quality of aluminum grooves over those generated using conventional PMD-Al processes. The present method inhibits PVD-Al migration and grain growth, which results in preventing abnormal patterning in the semiconductor device.